**Lab 5: Latches & Flip-Flops**

**ITI 1100 C – Digital Systems 1**

**Winter 2016**

**School of Electrical Engineering and Computer Science**

**University of Ottawa**

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Experiment Date: 2016-03-22

Submission Date: 2016-03-29

**Lab 5: Latches and Flip-Flops**

**Objectives**

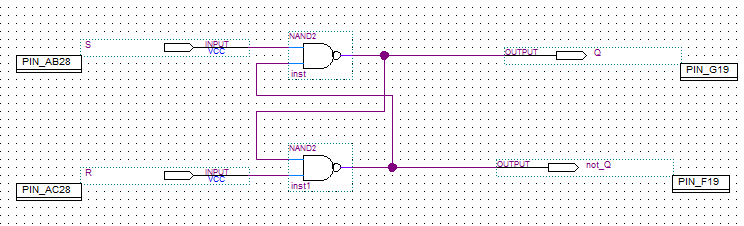
* Provide insight into the characteristics of several important latches and flip-flops
* Build latches and flip-flops from basic gates
* Explain concepts of latching and edge-triggering
* Test latches and flip-flops to understand their operation

**Equipment and Components**

* Quartus II 13.0 Service-Pack 1 Software (64-bit)
* Altera DE2-115 circuit board

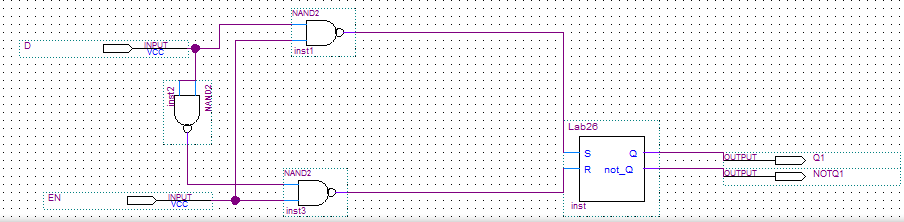
**Circuit Diagrams**

**Part 1 – SR Latch**

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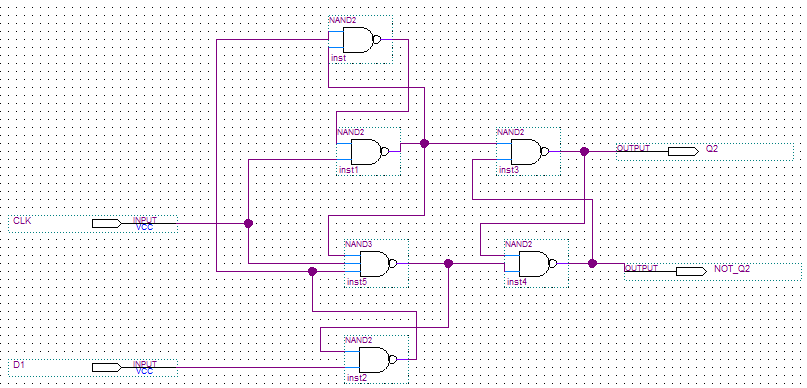
**Figure 1.1:** Screen-shot of the SR Latch circuit diagram.

**Part II – D Latch**

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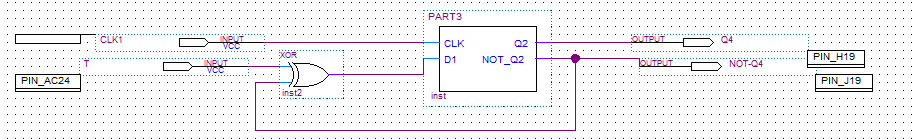
**Figure 2.1:** Screen-shot of the D Latch circuit diagram.

**Part III – D Flip-Flop**



**Figure 3.1:** Screen-shot of the D Flip-Flop circuit diagram.

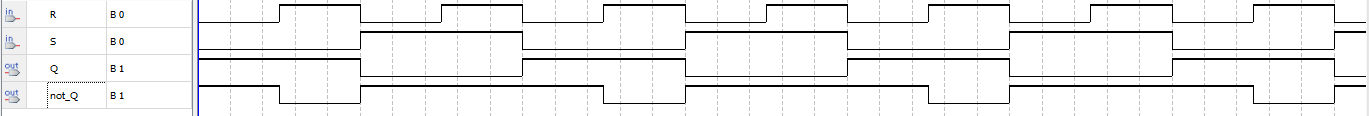
**Part IV – T Flip-Flop**



**Figure 4.1:** Screen-shot of the T Flip-Flop circuit diagram.

**Experimental Data and Data Processing**

**Part I – SR Latch**



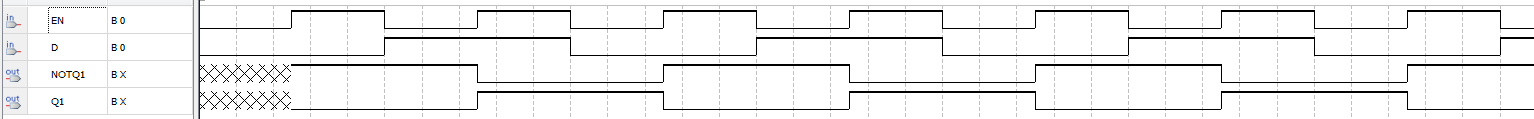
**Figure 1.2:** Screen-shot of the simulation output of the SR Latch circuit.

|  |  |  |
| --- | --- | --- |
| **S** | **R** | **Action** |
| 1 | 1 | Output does not change from the previous state. |
| 1 | 0 | RESET |
| 0 | 1 | SET |
| 0 | 0 | Forbidden condition: cannot store at the same time both 1 and 0 |

**Table 1.3:** Truth table for the SR Latch.

**Note:** Our waveform is the opposite to the one illustrated in the lab manual.

**Part II – D Latch**

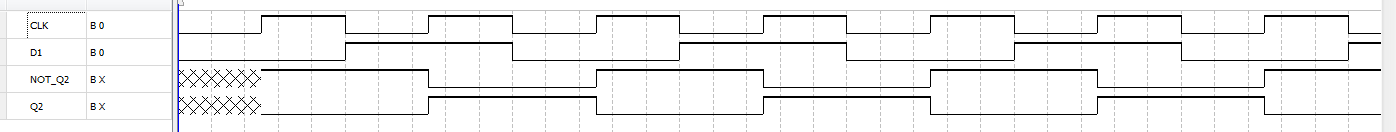
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**Figure 2.2:** Screen-shot of the simulation output of the D Latch circuit.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **EN** | **D** | **Q t + 1** | **(Q t + 1)’** | **Action** | **Comment** |
| 0 | x | Qt | (Qt)’ | Output does not change from the previous state. | Store |
| 1 | 0 | 0 | 1 | RESET | Transparent |
| 1 | 1 | 1 | 0 | SET |

**Table 2.3:** Truth table for the D Latch circuit.

**Part III – D Flip-Flop**

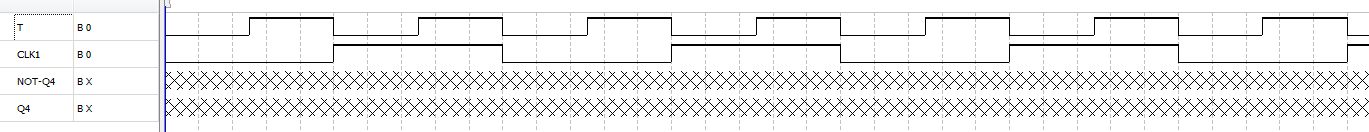


**Figure 3.2:** Screen-shot of the simulation output of the D Flip-Flop circuit.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLK** | **D** | **Qt + 1** | **(Q t + 1)’** | **Function** |
| ↑ | 0 | 0 | 1 | RESET |
| ↑ | 1 | 1 | 0 | SET |
| 0 | X | Qt | (Q t)’ | Inhibited |
| 1 | X | Qt | (Q t)’ | Inhibited |

**Table 3.3:** Truth table of positive edge triggered type D latch.

**Part IV – T Flip-Flop**

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**Figure 4.2:** Screen-shot of the simulation output of the T Flip-Flop.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **T** | **Qt +1** | **(Qt + 1)’** | **SET** | **RESET** |
| - | 0 | 0 | 0 | 1 |
| - | 0 | 1 | 1 | 0 |
| - | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 |

**Table 4.3:** Excitation table for the T Flip-Flop.

**Comparison of Theoretical Data and Experimental Data**

**Part 1 – SR Latch**

|  |  |  |  |
| --- | --- | --- | --- |
| **Inputs** | | **Expected Action** | **Actual Action** |
| **S** | **R** |
| 1 | 1 | Output does not change from the previous state. | Output does not change from the previous state. |
| 1 | 0 | RESET | RESET |
| 0 | 1 | SET | SET |
| 0 | 0 | Forbidden condition: cannot store at the same time both 1 and 0 | Forbidden condition: cannot store at the same time both 1 and 0 |

**Table 1.4:** Comparison of the theoretical and experimental results for the SR Latch circuit.

The results observed experimentally from the SR Latch circuit matched the theoretical actions.

**Part II – D Latch**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | **Expected Action** | **Actual Action** |
| **EN** | **D** | **Q t + 1** | **(Q t + 1)’** |
| 0 | x | Qt | (Qt)’ | Output does not change from the previous state. | Output does not change from the previous state. |
| 1 | 0 | 0 | 1 | RESET | RESET |
| 1 | 1 | 1 | 0 | SET | SET |

**Table 2.4:** Comparison of the theoretical and experimental results for the D Latch circuit.

The results observed experimentally from the D Latch circuit matched the theoretical actions.

**Part III – D Flip-Flop**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | **Expected Function** | **Actual Function** |
| **CLK** | **D** | **Qt + 1** | **(Q t + 1)’** |
| ↑ | 0 | 0 | 1 | RESET | RESET |
| ↑ | 1 | 1 | 0 | SET | SET |
| 0 | X | Qt | (Q t)’ | Inhibited | Inhibited |
| 1 | X | Qt | (Q t)’ | Inhibited | Inhibited |

**Table 3.4:** Comparison of the theoretical and experimental results of the D Flip-Flop circuit.

The results observed experimentally for the D Flip-Flop were identical to the theoretical functions.

**Part IV – T Flip-Flop**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Expected Outputs** | | | **Actual Outputs** | | | |
| **T** | **Qt +1** | **(Qt + 1)’** | **SET** | **RESET** | **SET** | **RESET** |
| - | 0 | 0 | 0 | 1 | 0 | 1 |
| - | 0 | 1 | 1 | 0 | 1 | 0 |
| - | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 |

**Table 4.4:** Comparison of the theoretical and experimental results of the T Flip-Flop circuit.

The results observed experimentally for the T Flip-Flop were identical to the theoretical functions.

**Discussion and Conclusions**

The objective of this experiment was to create, simulation and program an SR Latch, D latch, D Flip-Flop and T Flip-Flop circuit. We first predict the outcome theoretically by determining the output for every possible input combination. Then experimentally determine if our theoretical predictions are correct. The SR Latch is the simplest sequential circuit element. The D Latch has two operating modes that are controlled by the enable input – when the EN is active, the latch output follows the data input and when EN is inactive, the latch stores the data that was present when EN was last active. The D Flip-Flop circuit is a gated latch with a clock input. The Flip-Flop output changes when its clock input detects an edge (edge sensitive). A T Flip-Flop is a Flip-Flop whose output is between high and low on each clock pulse when input T is active. We did not have deviations from the expected results.